REMARKS

In view of the foregoing amendments and following remarks response to the Non-final Office Action dated June 5, 2007, Applicant respectfully requests favorable reconsideration of this application.

Claims 1-19 were pending in this application. Applicant has herein amended claims 1, 4, 6, 7, 12, 13, and 17, canceled claims 2, 5, 8, and 18, and added new claim 20, depending from claim 1. More particularly, Applicant has (1) amended independent claim 1 to add the limitations of former claim 2; (2) amended independent claim 7 to add the limitations of former claim 8, but to further limit the language to a transmitter switching topology (former claim 8 was worded to read on either a transmitter switch or a receiver switch); (3) amended independent claim 17 to add the limitations of former claim 18; and (4) slightly amended claims 4, 6, 12, and 13 to improve their form. Claims 2, 8, and 18 have been canceled.

Accordingly, claims 1, 3, 4, 6, 7, and 9-17, 19, and 20 are now pending in this application. Claims 1, 7, 14, and 17 are independent.

The Office rejected all of the claims, claims 1-19, as obvious over Gerlach in view of Yamamoto.

Applicant respectfully traverses. Particularly, independent claims 1, 14, and 17 each include a recitation that at least one of the switching topologies includes cascaded stages. Particularly, claim 1 recites that the receiver switching topology comprises "at least two cascaded stages, a first cascaded stage controllable to switch the transmission node to a receiver node, and a

second cascaded stage controllable to switch the receiver node to a selected one of the plurality of receiver ports". Claim 14 recites "at least some of the integrated circuit switching elements arranged in cascaded fashion in order to reduce signal insertion loss". Claim 17 recites "arranging at least some of the switching topologies in cascaded stages including a first stage coupled to the antenna port and a last stage coupled to a plurality of the transmitter or receiver ports".

The term "cascaded" in the specification refers to the type of topology illustrated in Figures 2 and 4 of the present application wherein the current path of a first transistor (e.g., transistor 19) (first cascaded stage) is coupled in series with the current paths of multiple transistors (e.g., transistors 20 and 22) (second cascaded stage).

In the specific embodiment described in the specification, for instance, transistor 19 of Figure 2 comprises the switch 108 in Figure 5 and transistors 20 and 22 comprise two of the four switches in switch 118 in Figure 5. As described in the specification, this cascaded topology, as opposed to the series topology of the prior art illustrated in Figure 1, decreases the insertion loss of the switching topology.

In the rejections, the Office relies on Yamamoto as teaching the cascaded aspect of the switching topology. (See the discussion in the Office Action of claim 2, which refers to Yamamoto, column 10, lines 25-67, and column 11, lines 1-2.) However, this portion of Yamamoto does not disclose a cascaded transistor configuration. Particularly, this portion of Yamamoto discusses Figure

7 of Yamamoto. Since it is unclear which portion of this discussion the Office believes discloses a cascade configuration, Applicant will briefly discuss both the transmitter portion and the receiver portion of Yamamoto and show that neither meets this limitation.

With respect to the transmitter portion, which is the circuitry on the left side of Figure 7 appearing between the transmitter 101 and the antenna 103, this arrangement is a cascode amplifier, i.e., comprising a common emitter transistor, F_1, and a common gate transistor, F_2. F_1 and F_2 are coupled in series. This is not a cascade. In fact, two transistors cannot form a cascade. It takes a minimum of three transistors to form a cascade.

Furthermore, note that, while these two series transistors are coupled in series, they are not coupled in series between the transmitter and the antenna, as claimed. The transmitter output is not coupled to one of the current path terminals of transistor F1, but to its gate. This configuration is not even properly considered a switch. It is an amplifier. Particularly, it is a cascode amplifier. Other than the fact that the word "cascode" sounds like the word "cascade", these two configurations are quite different from each other.

With respect to the receiver switching topology, which is shown on the right side of Figure 7 appearing between antenna 103 and receiver 102, it comprises three series-connected transistors, F_3, $F_{3'}$, and $F_{3''}$, between the antenna node 4 and an intermediate node 6 followed by a single transistor, F_4, coupled between the intermediate node 6 and ground.

Again, there is no cascade here. The three transistors F_3, $F_{3'}$, and $F_{3''}$ are coupled in series with each other, and therefore cannot possibly comprise the second (or subsequent) stage of a cascaded transistor switch (although this could form the first stage). Furthermore, the other transistor, F_4, is a single transistor, and therefore also could not possibly form the second (or subsequent) stage of a cascaded transistor switch. Furthermore, it is not even coupled in the path between the receiver 102 and the antenna 103. Therefore F_3, $F_{3'}$, and $F_{3''}$ could not form a cascade with F_4, whose current path is coupled between the node 6 and ground, not between the node 6 and the receiver 102.

Moreover, on both the transmitter side and the receiver side in Figure 7 of Yamamoto, there is only one transmitter node and one receiver node. Therefore, Yamamoto Figure 7 could not even possibly disclose a cascade arrangement between multiple transmitter or receiver nodes, on the one hand, and a port, on the other hand.

Accordingly, independent claims 1, 14, and 17 clearly patentably distinguish over the prior art of record.

Dependent claims 3, 4, 6, and 14-20 distinguish over the prior art for at least all of the reasons as the independent claims from which they depend. However, the dependent claims even further distinguish over the prior art of record.

For instance, newly amended dependent claim 4 depends from claim 1 and even further distinguishes over the prior art of record. Specifically, claim 4 adds that each transmitter switching section includes a series FET switching

topology comprising "a plurality of transistors with their current paths coupled in series between an associated transmission port and the transmission node". While transistors F_1 and F_2 in the transmitter switching topology of Yamamoto Figure 7 might be considered to be coupled in series, they certainly are not coupled in series between the transmission port and the transmission node. As previously noted, this is a cascode amplifier configuration in which the output of the transmitter is coupled to the gate terminal of F_1, not to one of its current path terminals.

Dependent claim 6 depends from claim 1 and even further distinguishes over the prior art of record. It recites that at least one of the FETs has "a plurality of contiguous source regions interdigitated with a plurality of contiguous drain regions, a sinuous gate formed to wind between the source regions and the gate regions". The Office asserts that this is found in Yamamoto at column 5, lines 57-67, column 6, lines 1-9, and column 11, lines 3-61. However, these portions of Yamamoto do not discuss at all the layout of the transistors themselves, and, thus are entirely irrelevant.

Dependent claim 15 depends from claim 14 and further elaborates on the cascaded transistor configuration and, therefore, even further distinguished over the prior art of record.

Independent claim 7 distinguishes over the prior art of record for all the reasons discussed above in connection with dependent claim 4. Particularly, both claim 4 and claim 7 recite that at least one of the transmitter switching

topologies comprises a plurality of field effect transistors with their current paths coupled in series between an associated transmission port and the antenna port.

Dependent claim 9 depends from claim 7 and includes essentially the same limitations discussed above in connection with dependent claim 6. Accordingly, it even further distinguishes over the prior art of record for at least all of the same additional reasons discussed above in connection with dependent claim 6.

Dependent claim 10 depends from claim 7 and adds the limitation that the transmitter port switching topologies occupy an area on the die substantially larger than the receiver port switching topologies. The Office asserted that this is found in Yamamoto at column 11, lines 3-23 and 51-67. However, these portions of Yamamoto have nothing whatsoever to do with the transistor layout. Accordingly, not only do they not disclose what is claimed in claim 10, they are irrelevant to claim 10.

In view of the foregoing remarks, this application is now in condition for allowance. Applicant respectfully requests the Office to issue a Notice of Allowance at the earliest possible date. The Examiner is invited to contact

Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

Respectfully submitted,

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